Advanced

# GT24C2048H

# Industrial 2048-Kbit I2C Bus EEPROM

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## 1. Features

- Two-Wire Serial Interface, I²C™ Compatible
  - Bi-directional data transfer protocol
- Wide-voltage Operation
  - $V_{CC}$ = 1.7V to 3.6V
- Speed: 1 MHZ (1.7V ~ 3.6V)
- Standby current (max.): 3 μA, 3.6V
- Operating current (max.): 2 mA, 3.6V
- Sequential & Random Read Features
- Memory organization: 2048Kb (262,144 x 8)
- Page Size: 256 bytes
- Page write mode
  - Partial page writes allowed
  - Addition write lockable page (Identification Page)
- Self-timed write cycle: 5 ms (max.)
- Endurance:
  - ✧ 4 million Write cycles at 25 °C
- Data retention
  - ✧ 100 years at 25 °C
- Packages: SOIC, TSSOP, UDFN
- ESD Protection > 4000V
- Lead-free, RoHS, Halogen free, Green
- Noise immunity on inputs, besides Schmitt trigger

## 2. General Description

The GT24C2048H is a 2048-Kbit serial EEPROM Industrial grade device operating up to 85°C. The GT24C2048H contains a memory array of 2048K bits (262,144 x8), which is organized in 256-byte per page.

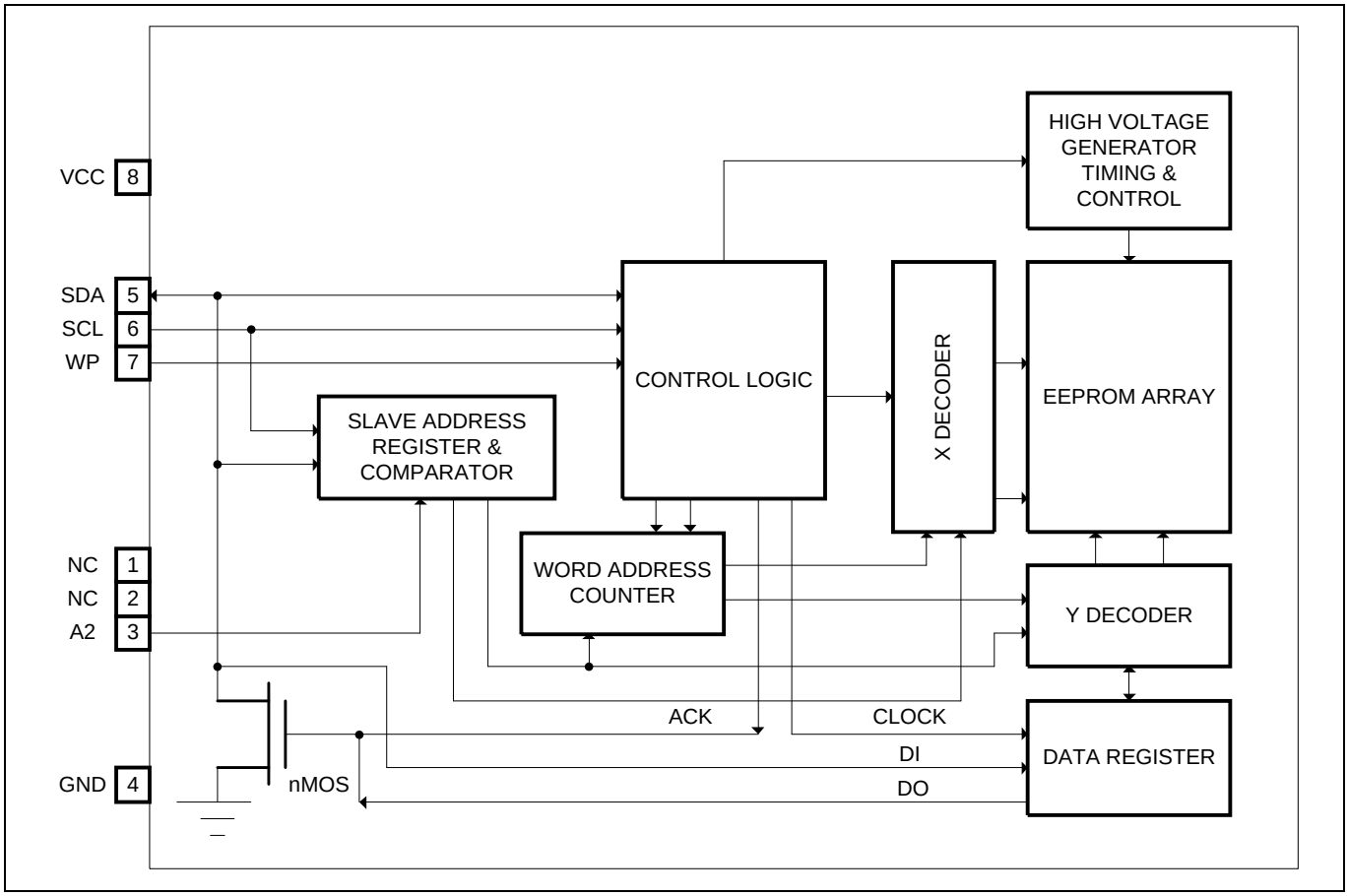
The EEPROM operates in a wide voltage range from 1.7V to 3.6V running up to 1MHz, which fits most application. The product provides low-power operations and low standby current. The device is offered in Lead-free, RoHS, halogen free or Green package. The available package types are 8-pin SOIC, TSSOP, UDFN.

The GT24C2048H is compatible to the standard I²C bus protocol. The simple bus consists of Serial Clock (SCL) and Serial Data (SDA) signals. Utilizing such bus protocol, a Master device, such as a microcontroller, can usually control one or more Slave devices, alike this GT24C2048H. The bit stream over the SDA line includes a series of bytes, which identifies a particular Slave device, an instruction, an address within that Slave device, and a series of data, if appropriate. The GT24C2048H also has a Write Protect function via WP pin to cease from overwriting the data stored inside the memory array.

In order to refrain the state machine from entering into a wrong state during power-up sequence or a power toggle off-on condition, a power on reset circuit is embedded. During power-up, the device does not respond to any instructions until the supply voltage ($V_{CC}$) has reached an acceptable stable level above the reset threshold voltage. Once $V_{CC}$ passes the power on reset threshold, the device is reset and enters into the Standby mode. This would also avoid any inadvertent Write operations during power-up stage. During power-down process, the device will enter into standby mode, once $V_{CC}$ drops below the power on reset threshold voltage. In addition, the device will be in standby mode after receiving the Stop command, provided that no internal write operation is in progress. Nevertheless, it is illegal to send a command unless the $V_{CC}$ is within its operating level.

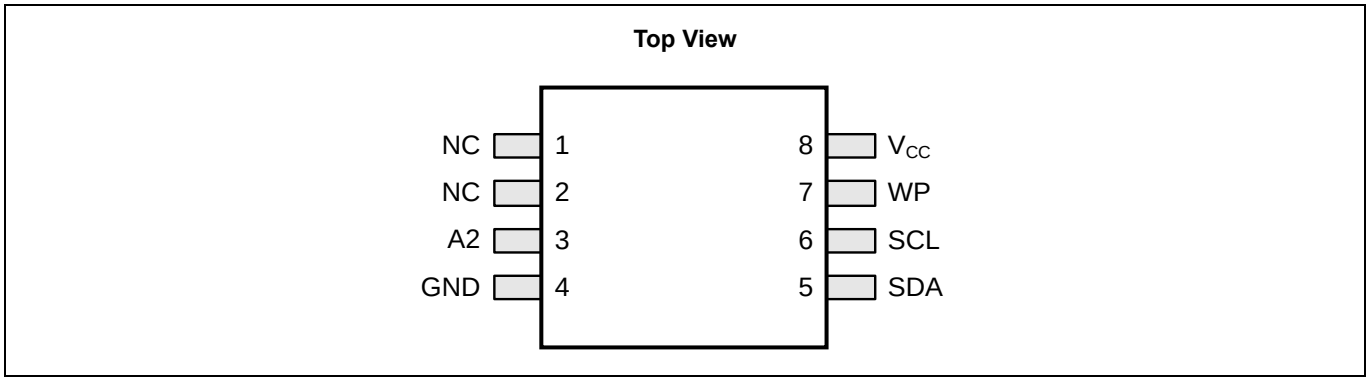
This product optionally offers an additional page (Identification Page) of 256 bytes. The Identification Page can be used to store sensitive application parameters which can be (later) permanently locked in Read-only mode.

## 3. Functional Block Diagram

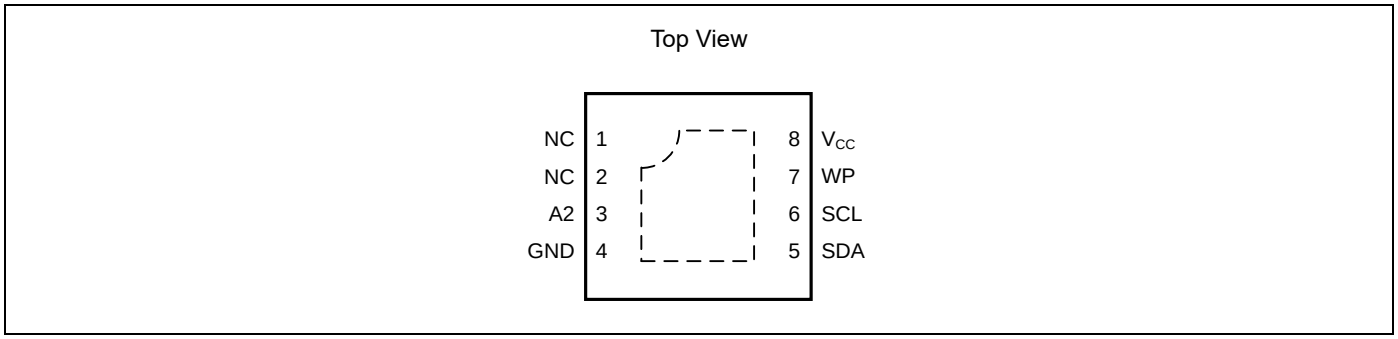


## 4. Pin Configuration

### 4.1 8-Pin SOIC, TSSOP




### 4.2 8-Lead UDFN




### 4.3 Pin Definition

| Pin No. | Pin Name | I/O | Definition |
|---|---|---|---|
| 1 | NC | - | Not connected |
| 2 | NC | - | Not connected |
| 3 | A2 | I | Device Address Input |
| 4 | GND | - | Ground |
| 5 | SDA | I/O | Serial Address, Data input and Data output |
| 6 | SCL | I | Serial Clock Input |
| 7 | WP | I | Write Protect Input |
| 8 | $V_{CC}$ | - | Power Supply |

### 4.4 Pin Descriptions

#### SCL

This input clock pin is used to synchronize the data transfer to and from the device.

**SDA**

The SDA is a bi-directional pin used to transfer addresses and data into and out of the device. The SDA pin is an open drain output and can be wired with other open drain or open collector outputs. However, the SDA pin requires a pull-up resistor connected to the power supply.

**WP**

WP is the Write Protect pin. While the WP pin is connected to the power supply of GT24C2048H, the entire array becomes Write Protected (i.e. the device becomes Read only). When WP is tied to Ground or left floating, the normal write operations are allowed.
Note: The voltage of WP pin can‘t rise earlier than Vcc.

**A2**

The A2 is the device address input.

Typically, the A2 pin is for hardware addressing and a total of 2 devices can be connected on a single bus system. When A2 is left floating, the input is defaulted to zero.

**$V_{CC}$**

Supply voltage

**GND**

Ground of supply voltage

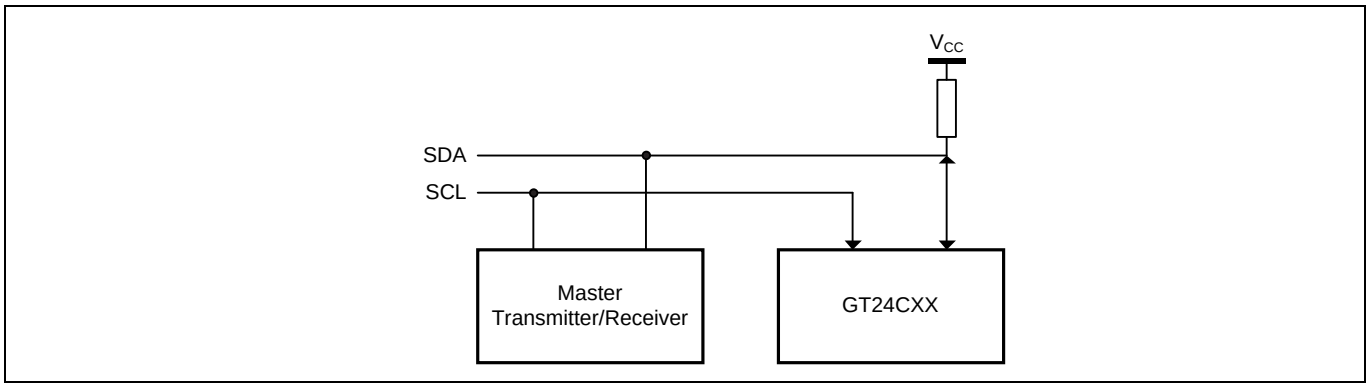
## 5. Device Operation

The GT24C2048H serial interface supports communications using the standard 2-wire bus protocol, such as $I^2C$.

### 5.1 2-WIRE Bus

The two-wire bus is defined as Serial Data (SDA), and Serial Clock (SCL). The protocol defines any device that sends data onto the SDA bus as a transmitter, and the receiving devices as receivers. The bus is controlled by Master device that generates the SCL, controls the bus access, and generates the Start and Stop conditions. The GT24C2048H is the Slave device.

***Figure 1. Typical System Bus Configuration***

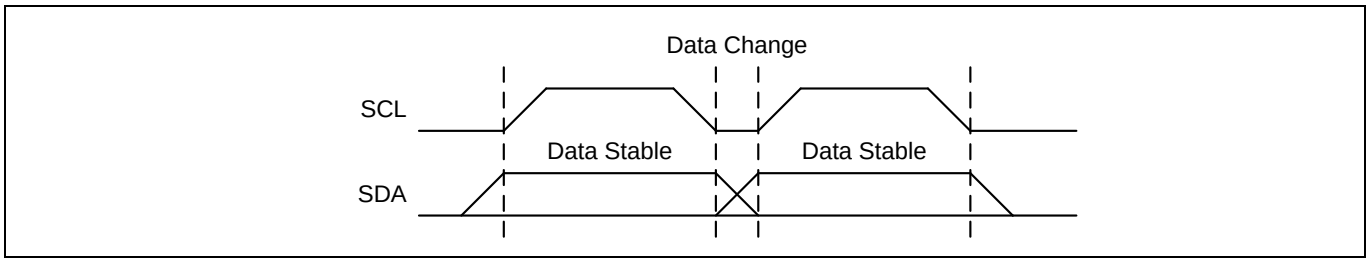



### 5.2 The Bus Protocol

Data transfer may be initiated only when the bus is not busy. During a data transfer, the SDA line must remain stable whenever the SCL line is high. Any changes in the SDA line while the SCL line is high will be interpreted as a Start or Stop condition.

The state of the SDA line represents valid data after a Start condition. The SDA line must be stable for the duration of the High period of the clock signal. The data on the SDA line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a Start condition and terminated by a Stop condition.

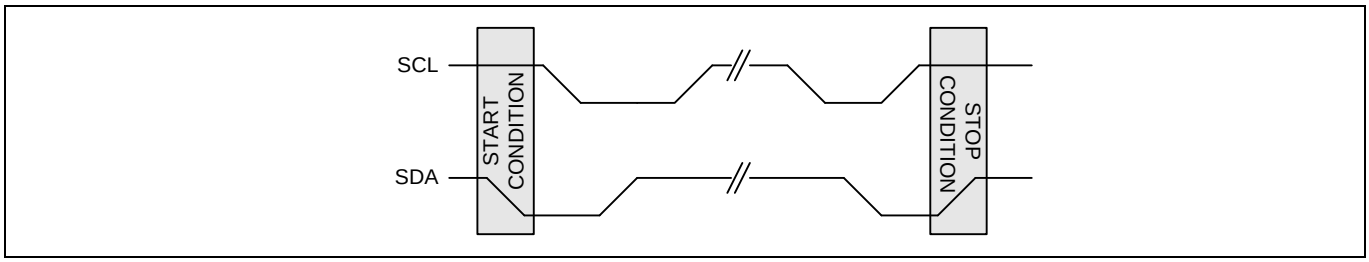
***Figure 2. Data Validity Protocol***




### 5.3 Start Condition

The Start condition precedes all commands to the device and is defined as a High to Low transition of SDA when SCL is High. The EEPROM monitors the SDA and SCL lines and will not respond until the Start condition is met.

***Figure 3. Start and Stop Conditions***



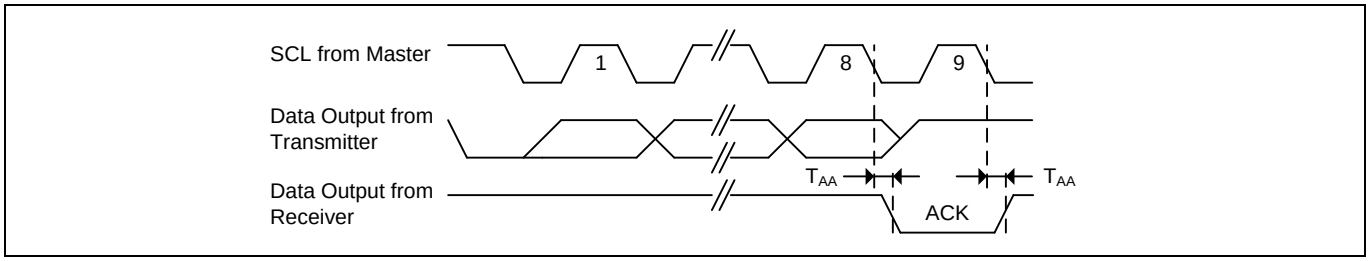

### 5.4 Stop Condition

The Stop condition is defined as a Low to High transition of SDA when SCL is High. All operations must end with a Stop condition.

### 5.5 Acknowledge

After a successful data transfer, each receiving device is required to generate an ACK. The Acknowledging device pulls down the SDA line.

***Figure 4. Output Acknowledge***




### 5.6 Reset

The GT24C2048H contains a reset function in case the 2-wire bus transmission on is accidentally interrupted (e.g. a power loss), or needs to be terminated mid-stream. The reset is initiated when the Master device creates a Start condition. To do this, it may be necessary for the Master device to monitor the SDA line while cycling the SCL up to nine times. (For each clock signal transition to High, the Master checks for a High level on SDA.) In the event that the device is still non-responsive or remains active on the SDA bus, a power cycle must be used to reset the device.

### 5.7 Standby Mode

While in standby mode, the power consumption is minimal. The GT24C2048H enters into standby mode during one of the following conditions: a) After Power-up, while no Op-code is sent; b) After the completion of an operation and followed by the Stop signal, provided that the previous operation is not Write related; or c) After the completion of any internal write operations.

### 5.8 Device Addressing

The Master begins a transmission on by sending a Start condition, then sends the address of the particular Slave devices to be communicated. The Slave device address is 8 bits format as shown in Figure 5.

The four most significant bits of the Slave address are fixed (1010) for GT24C2048H.

The next bit, A2, of the Slave address is specifically related to EEPROM. Up to 2 GT24C2048H units can be connected to the 2-wire bus.

The bit2 and bit1 are the memory page address A[17] and A[16].

The last bit of the Slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, Read operation is selected. While it is set to 0, Write operation is selected.

After the Master transmits the Start condition and Slave address byte appropriately, the associated 2-wire Slave device, GT24C2048H, will respond with ACK on the SDA line. Then GT24C2048H will pull down the SDA on the ninth clock cycle, signaling that it received the eight bits of data.

The GT24C2048H then prepares for a Read or Write operation by monitoring the bus.

***Figure 5. Device Address***

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Main Array | 1 | 0 | 1 | 0 | A2 | A[17] | A[16] | R/$\overline{W}$ |
| ID Page | 1 | 0 | 1 | 1 | A2 | X | X | R/$\overline{W}$ |

Note: ID page is optional for different part number.

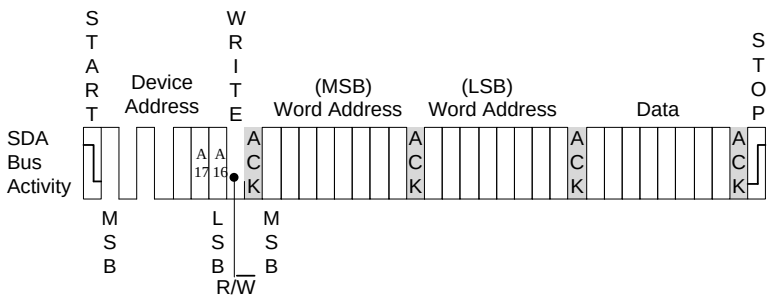
## 5.9 Write Operation

Access each data in the memory requires an 18-bit address. The Most significant bits A[17] and A[16] are in the device address and the Least Significant Bits A[15:0] are defined in two address bytes. The most significant word address followed by the least significant word address.

### 5.9.1 Byte Write

In the Byte Write mode, the Master device sends the Start condition and the Slave address information (with the R/W set to Zero) to the Slave device. After the Slave generates an ACK, the Master sends the byte address that is to be written into the address pointer of the GT24C2048H. After receiving another ACK from the Slave, the Master device transmits the data byte to be written into the address memory location. The GT24C2048H acknowledges once more and the Master generates the Stop condition, at which time the device begins its internal programming cycle. While this internal cycle is in progress, the device will not respond to any request from the Master device.

***Figure 6. Byte Write***

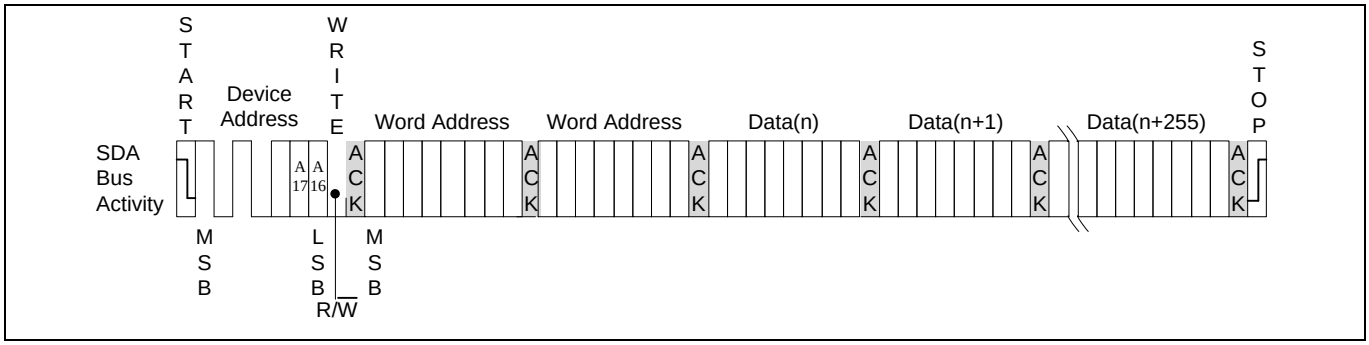



### 5.9.2 Page Write

The GT24C2048H is capable of 256-byte Page-Write operation. A Page-Write is initiated in the same manner as a Byte Write, but instead of terminating the internal Write cycle after the first data byte is transferred, the Master device can transmit up to 255 more bytes. After the receipt of each data byte, the EEPROM responds immediately with an ACK on SDA line, and the eight lower order data byte address bits are internally incremented by one, while the higher order bits of the data byte address remain constant. If

a byte address is incremented from the last byte of a page, it returns to the first byte of that page. If the Master device should transmit more than 256 bytes prior to issuing the Stop condition, the address counter will “roll over,” and the previously written data will be overwritten. Once all 256 bytes are received and the Stop condition has been sent by the Master, the internal programming cycle begins. At this point, all received data is written to the GT24C2048H in a single Write cycle. All inputs are disabled until completion of the internal Write cycle.

***Figure 7. Page Write***




### 5.9.3 Acknowledge (ACK) Polling

The disabling of the inputs can be used to take advantage of the typical Write cycle time. Once the Stop condition is issued to indicate the end of the host's Write operation, the GT24C2048H initiates the internal Write cycle. ACK polling can be initiated immediately. This involves issuing the Start condition followed by the Slave address for a Write operation. If the EEPROM is still busy with the Write operation, no ACK will be returned. If the GT24C2048H has completed the Write operation, an ACK will be returned and the host can then proceed with the next Read or Write operation.

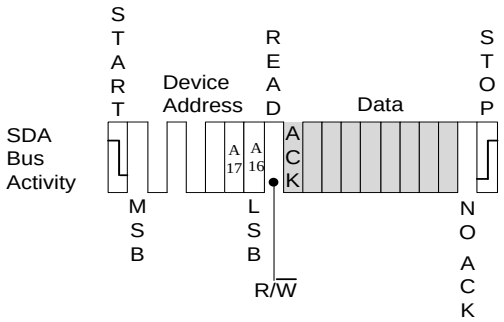
## 5.10 Read Operation

Read operations are initiated in the same manner as Write operations, except that the (R/W) bit of the Slave address is set to “1”. There are three Read operation options: current address read, random address read and sequential read.

### 5.10.1 Current Address Read

The GT24C2048H contains an internal address counter which maintains the address of the last byte accessed, incremented by one. For example, if the previous operation is either a Read or Write operation addressed to the address location n, the internal address counter would increment to address location n+1. When the EEPROM receives the Slave Addressing Byte with a Read operation (R/W bit set to “1”), it will respond an ACK and transmit the 8-bit data byte stored at address location n+1. The Master should not acknowledge the transfer but should generate a Stop condition so the GT24C2048H discontinues transmission. If 'n' is the last byte of the memory, the data from location '0' will be transmitted. (Refer to Figure 8. Current Address Read Diagram.)

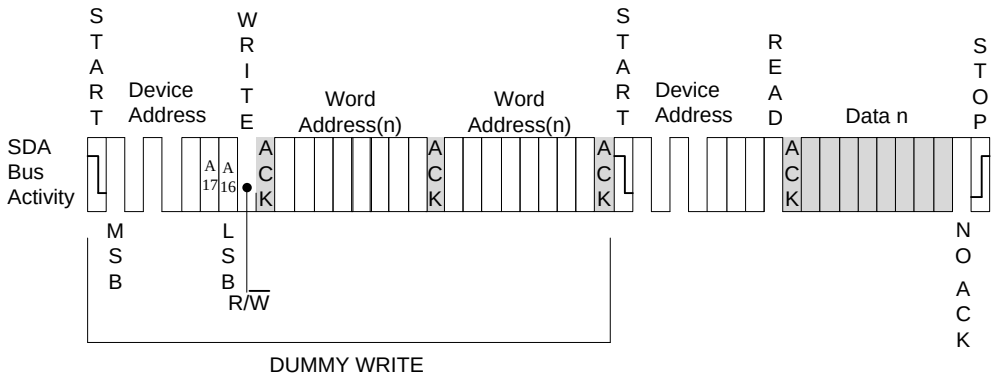
***Figure 8. Current Address Read***




### 5.10.2 Random Address Read

Selective Read operations allow the Master device to select at random any memory location for a Read operation. The Master device first performs a 'dummy' Write operation by sending the Start condition, Slave address and byte address of the location it wishes to read. After the GT24C2048H acknowledges the byte address, the Master device resends the Start condition and the Slave address, this time with the R/W bit set to one. The EEPROM then responds with its ACK and sends the data requested. The Master device does not send an ACK but will generate a Stop condition. (Refer to Figure 9. Random Address Read Diagram.)

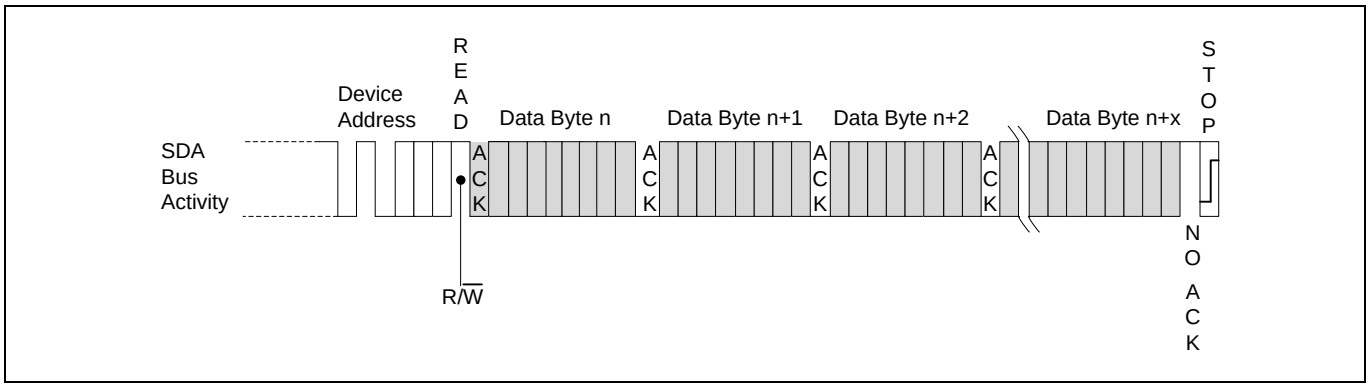
***Figure 9 Random Address Read***




### 5.10.3 Sequential Read

Sequential Reads can be initiated as either a Current Address Read or Random Address Read. After the GT24C2048H sends the initial byte sequence, the Master device now responds with an ACK indicating it requires additional data from the GT24C2048H. The EEPROM continues to output data for each ACK received. The Master device terminates the sequential Read operation by pulling SDA High (no ACK) indicating the last data byte to be read, followed by a Stop condition. The data output is sequential, with the data from address n followed by the data from address n+1, n+2 ... etc. The address counter increments by one automatically, allowing the entire memory contents to be serially read during sequential Read operation. When the memory address boundary of the array is reached, the address counter “rolls over” to address 0, and the device continues to output data. (Refer to Figure 10. Sequential Read Diagram).

***Figure 10. Sequential Read***




## 5.11 Identification Page

The GT24C2048H optionally offers an additional Identification Page (256 bytes) in addition to the 2048-Kbit memory.

### 5.11.1 Write Identification Page

The Identification Page (256 byte) is an additional page which can be written and (later) permanently locked in Read-only mode. It is written by issuing the Write Identification Page instruction. This instruction uses the same protocol and format as Page Write (into memory array), except for the following differences:

- Device type identifier = 1011b
- MSB address bits A[17:8] are don't care except for address bit A10 which must be '0'. LSB address bits A[7:0] define the byte address inside the Identification page.

If the Identification page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (NoAck).

### 5.11.2 Lock Identification Page

The Lock Identification Page instruction (Lock ID) permanently locks the Identification page in Read-only mode. The lock ID instruction is similar to Byte Write (into memory array) with the following specific condition:

- Device type identifier=1011b
- Address bit A10 must be '1'; all other address bits are don't care
- The data byte must be equal to the binary value xxxx xx1x, where x is don't care

### 5.11.3 Read Identification Page

The Identification Page (256 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode.

The Identification Page can be read by issuing an Read Identification Page instruction. This instruction uses the same protocol and format as the Random Address Read (from memory array) with device type identifier defined as 1011b. The MSB address bits A[17:8] are don't care, the LSB address bits A[7:0] define the byte address inside the Identification Page. The number of bytes to read in the ID page must not exceed the page boundary (e.g.: when reading the Identification Page from location 100d, the number of bytes should be less than or equal to 156, as the ID page boundary is 256 bytes).

### 5.11.4 Read the lock status

The locked/unlocked status of the Identification page can be checked by transmitting a specific truncated command [Identification

Page Write instruction + one data byte] to the device. The device returns an acknowledge bit if the Identification page is unlocked, otherwise a NoAck bit if the Identification page is locked.

Right after this, it is recommended to transmit to the device a start followed by a Stop condition, so that:

- Start: the truncated command is not executed because the Start condition resets the device internal logic.
- Stop: the device is then set back into Standby mode by the Stop condition.

### 5.12 Delivery State

GT24C2048H is shipped erased status with all bytes value as FFh.

# 6. Application Recommendation

## 6.1 Operating Supply Voltage

Prior to selecting the memory and issuing instructions to it, a valid and stable VCC voltage within the specified [VCC(min), VCC(max)] range must be applied. This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal Write cycle (tW).

In order to filter out small ripples on VCC, it is recommended to connect a decoupling capacitor (typically 0.1μf) between VCC and GND. In addition, it is recommended to tie the pull-up resistor to the same VCC power source as EEPROM, if MCU is powered by a different VCC power source.

## 6.2 Power-up conditions

During power ramp up, once VCC level reaches the power on reset threshold, the EEPROM internal logic is reset to a known state. While VCC reaches the stable level above the minimum operation voltage, the EEPROM can be operated properly. Therefore, in a good power on reset, VCC should always begin at 0V and rise straight to its normal operating level, instead of being at an uncertain level. Only after a good power on reset, can EEPROM work normally.

At power-up, the device does not respond to any instruction until VCC reaches the internal threshold voltage (this threshold is defined in the DC characteristic Table as $V_{RES}$).

When VCC passes over the POR threshold, the device is reset and in the following state:

- in the Standby power mode
- deselected

As soon as the VCC voltage has reached a stable value within the [VCC(min), VCC(max)] range, the device is ready for operation.

## 6.3 Power-down

During power-down (continuous decrease in the VCC supply voltage below the minimum VCC operating voltage), the device must be in Standby power mode (that is after a STOP condition or after the completion of the Write cycle tW if an internal Write cycle is in progress).

## 6.4 ECC (Error Correction Code) and Write cycling

The Error Correction Code (ECC) is an internal logic function which is transparent for the I2C communication protocol.

If a single bit out of a byte happens to be erroneous during a Read operation, the ECC detects this bit and replaces it with the correct value. The read reliability is therefore much improved.

# 7. Electrical Characteristics

## 7.1 Absolute Maximum Ratings

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_S$ | Supply Voltage | -0.5 to Vcc+1 | V |
| $V_P$ | Voltage on Any Pin | –0.5 to Vcc+1 | V |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |
| $I_{OUT}$ | Output Current | 5 | mA |
| $V_{ESD}$ | Electrostatic pulse (Human Body model) | >4000 | V |

Note: Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## 7.2 Operating Range

| Range | Ambient Temperature ($T_A$) | $V_{CC}$ |
|---|---|---|
| Industrial | –40°C to +85°C | 1.7V to 3.6V |

## 7.3 Capacitance

| Symbol | Parameter[1, 2] | Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 6 | pF |
| $C_{I/O}$ | Input / Output Capacitance | $V_{I/O}$ = 0V | 8 | pF |

Notes: [1] Tested initially and after any design or process changes that may affect these parameters and not 100% tested.

[2] Test conditions: $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 3.6V.

## 7.4 Reliability

| Symbol | Parameter | Condition | Min. | Unit |
|---|---|---|---|---|
| End | Endurance | Ta=+25°C | 4 million | Program / Erase Cycles |
| DR | Data Retention | Ta=+25°C | 100 | Years |

### 7.5 DC Electrical Characteristic

| Symbol | Parameter [1] | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | 1.7 | | 3.6 | V |
| $V_{IH}$ | Input High Voltage( WP, A0, A1, A2) | | 0.7*$V_{CC}$ | | $V_{CC}$+0.5 | V |
| | Input High Voltage( SCL and SDA ) | | 0.7*$V_{CC}$ | | $V_{CC}$+0.5 | |
| $V_{IL}$ | Input Low Voltage | | -0.5 | | 0.3* $V_{CC}$ | V |
| $I_{LI}$ | Input Leakage Current | Vcc=3.6V,$V_{IN}$ = $V_{CC}$ max | — | | 2 | μA |
| $I_{LO}$ | Output Leakage Current | Vcc=3.6V | — | | 2 | μA |
| $V_{OL1}$ | Output Low Voltage | Vcc=1.7V,$I_{OL}$ = 1.5 mA | — | | 0.2 | V |
| $V_{OL2}$ | Output Low Voltage | Vcc=2.5V,$I_{OL}$ = 2.1 mA | — | | 0.4 | V |
| $I_{SB1}$ | Standby Current | Vcc=1.7V,$V_{IN}$ = $V_{CC}$ or GND | — | 0.5 | 1 | μA |
| $I_{SB2}$ | Standby Current | Vcc=2.5V,$V_{IN}$ = $V_{CC}$ or GND | — | 1 | 2 | μA |
| $I_{SB3}$ | Standby Current | Vcc=3.6V,$V_{IN}$ = $V_{CC}$ or GND | — | 1.5 | 3 | μA |
| $I_{CC1}$ | Read Current | Vcc=1.7V,Read at 400 KHz | — | | 1 | mA |
| | | Vcc=2.5V,Read at 400 KHz | | | 1 | mA |
| | | Vcc=3.6V,Read at 400 KHz | — | | 1 | mA |
| | | Vcc=1.7V,Read at 1 MHz | | | 2 | mA |
| | | Vcc=2.5V,Read at 1 MHz | | | 2 | mA |
| | | Vcc=3.6V,Read at 1 MHz | — | | 2 | mA |
| $I_{CC2}$ | Write Current | During tWR | | | 5 | mA |
| $V_{RES}$ | Internal reset threshold voltage | | 0.5 | | 1.5 | V |

### 7.6 AC Electrical Characteristic

| Symbol | Parameter [1] [2] | 1.7V≤Vcc≤3.6V Slow Mode | | 1.7V≤Vcc≤3.6V Fast Mode | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $F_{SCL}$ | SCK Clock Frequency | | 400 | | 1000 | KHz |
| $T_{LOW}$ | Clock Low Period | 1200 | — | 500 | — | ns |
| $T_{HIGH}$ | Clock High Period | 600 | — | 260 | — | ns |
| $T_R$ | Rise Time (SCL and SDA) | — | 300 | — | 120 | ns |
| $T_F$ | Fall Time (SCL and SDA) | — | 300 | — | 120 | ns |
| $T_{SU:STA}$ | Start Condition Setup Time | 500 | — | 200 | — | ns |
| $T_{SU:STO}$ | Stop Condition Setup Time | 500 | — | 200 | — | ns |
| $T_{HD:STA}$ | Start Condition Hold Time | 500 | — | 200 | — | ns |
| $T_{SU:DAT}$ | Data In Setup Time | 100 | — | 40 | — | ns |
| $T_{HD:DAT}$ | Data In Hold Time | 0 | — | 0 | — | ns |
| $T_{AA}$ | Clock to Output Access time (SCL Low to SDA Data Out Valid) | 100 | 900 | 50 | 400 | ns |
| $T_{DH}$ | Data Out Hold Time (SCL Low to SDA Data Out Change) | 100 | — | 50 | — | ns |
| $T_{WR}$ | Write Cycle Time | — | 5 | — | 5 | ms |
| $T_{BUF}$ | Bus Free Time Before New Transmission | 1000 | — | 400 | — | ns |
| T | Noise Suppression Time | — | 50 | — | 50 | ns |
| Endr | Endurance (3.6V, 25C, page mode) | 1 million | | | | cycles |

Notes: [1] The parameters are characterized but not 100% tested.

[2] AC measurement conditions:

$R_L$ (connects to $V_{CC}$): 1.3 kΩ (2.5V, 3.6V), 10 kΩ (1.7V)

$C_L$ = 100 pF

Input pulse voltages: 0.3*$V_{CC}$ to 0.7*$V_{CC}$

Input rise and fall times: ≤ 50 ns

Timing reference voltages: half $V_{CC}$ level

### 7.7 Timing Diagrams

***Figure 11. Bus Timing***

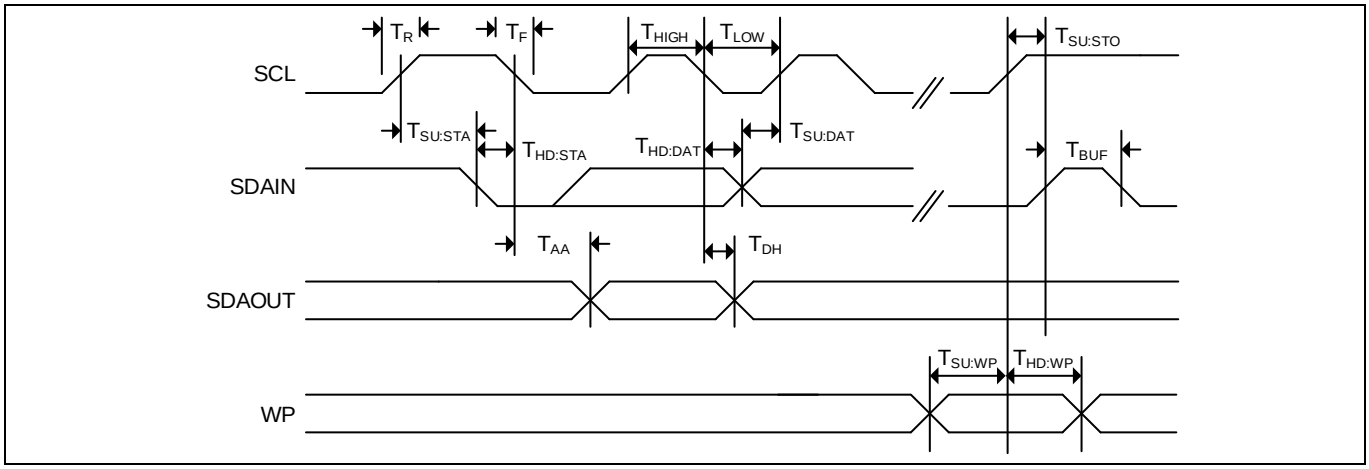
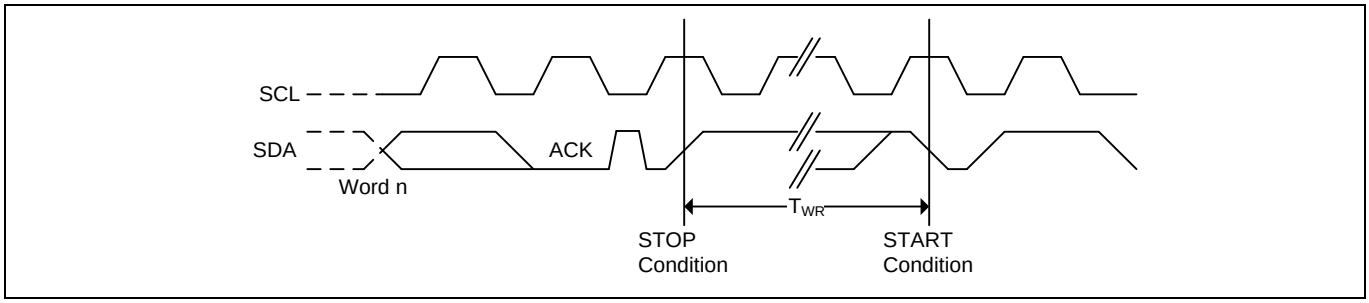



***Figure 12. Write Cycle Timing***



## 8. Ordering Information

| Voltage Range | Part Number* | Package (8-pin)* |
|---|---|---|
| 1.7V to 3.6V | GT24C2048H-4GLI-TR | 150-mil SOIC |
| | GT24C2048H-4ZLI-TR | 3 x 4.4 mm TSSOP |
| | GT24C2048H-4UDLI-TR | 2 x 3 x 0.55 mm UDFN |

**Rule:**

| |
|---|
| **Device Type** |
| **GT24C= I2C Protocol Industrial EEPROM** |
| **Device Density** |
| **2048H = 2048K-bit Product version H** |
| **Operating Voltage** |
| **4 = 1.7-3.6V** |
| **Package** |
| **G = SOP8 150mil** |
| **Z = TSSOP8** |
| **UD=UDFN 2*3mm** |
| **Pb Status** |
| **L = green status（HF, Meet reach, Rohs, etc.）** |
| **Temperature Range** |
| **I=Industrial(-40C ~ +85℃)** |
| **Packing** |
| **TR = Tape & Reel** |

Note:

1. Contact Giantec Sales Representatives for availability and other package information.
2. The product is packed in tape and reel “-TR”
3. Refer to Giantec website for related declaration document on lead free, RoHS, halogen free or Green, whichever is applicable.

## 9. Top Markings

### 9.1 SOIC package


***G***: Giantec Logo

42048H4GU: GT24C2048H-4GLI-TR

YWW: Date Code, Y=year, WW=week

### 9.2 TSSOP package


***GT***: Giantec Logo

42048H4ZU: GT24C2048H-4ZLI-TR

YWW: Date Code, Y=year, WW=week

### 9.3 UDFN package


**GT**: Giantec Logo

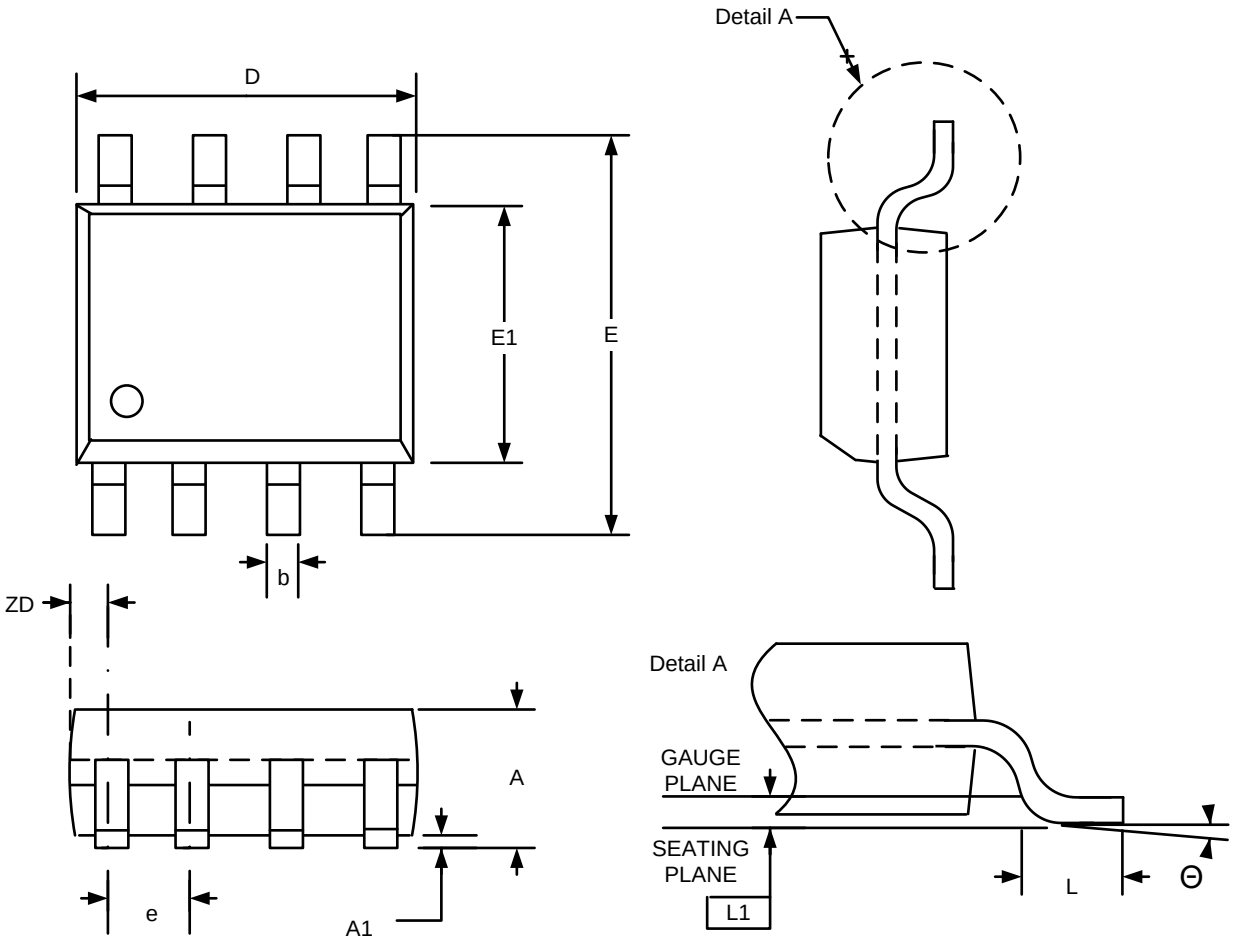
4BH: GT24C2048H-4UDLI-TR

YWW: Date Code, Y=year, WW=week

## 10. Package Information

### 10.1 SOIC

**8L 150mil SOIC Package Outline**

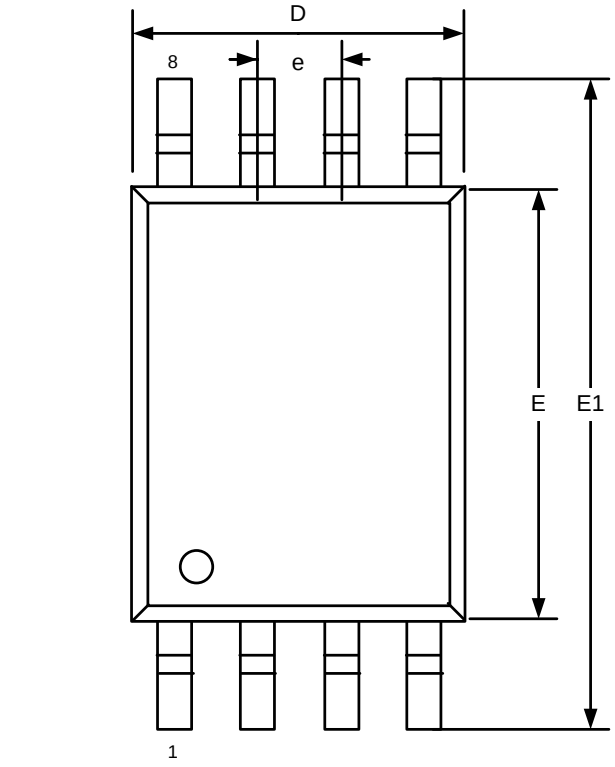


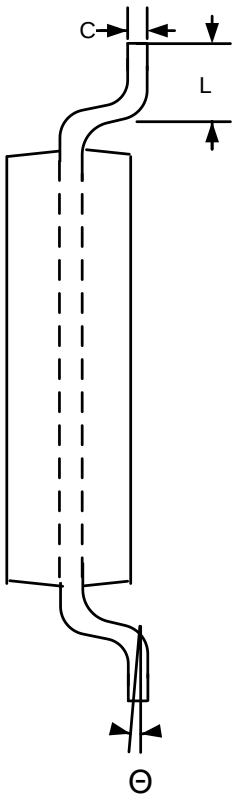

| SYMBOLS | DIMENSIONS IN MILLIMETERS | | | DIMENSIONS IN INCHES | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 1.35 | -- | 1.75 | 0.053 | -- | 0.069 |
| A1 | 0.10 | -- | 0.25 | 0.004 | -- | 0.010 |
| b | 0.33 | -- | 0.51 | 0.013 | -- | 0.020 |
| D | 4.80 | -- | 5.00 | 0.189 | -- | 0.197 |
| E | 5.80 | -- | 6.20 | 0.228 | -- | 0.244 |
| E1 | 3.80 | -- | 4.00 | 0.150 | -- | 0.157 |
| e | 1.27 BSC. | | | 0.050 BSC. | | |
| L | 0.38 | -- | 1.27 | 0.015 | | 0.050 |
| L1 | 0.25 BSC. | | | 0.010 BSC. | | |
| ZD | 0.545 REF. | | | 0.021 REF. | | |
| Θ | 0 | -- | 8° | 0 | -- | 8° |

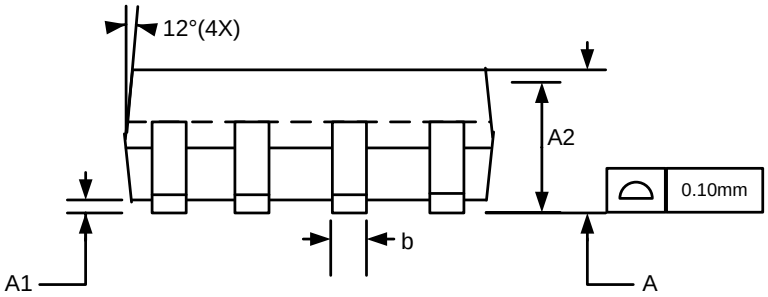
Note:
1. Controlling Dimension:MM
2. Dimension D and E1 do not include Mold protrusion
3. Dimension b does not include dambar protrusion/intrusion.
4. Refer to Jedec standard MS-012
5. Drawing is not to scale

## 10.2 TSSOP

### 8L 3x4.4mm TSSOP Package Outline



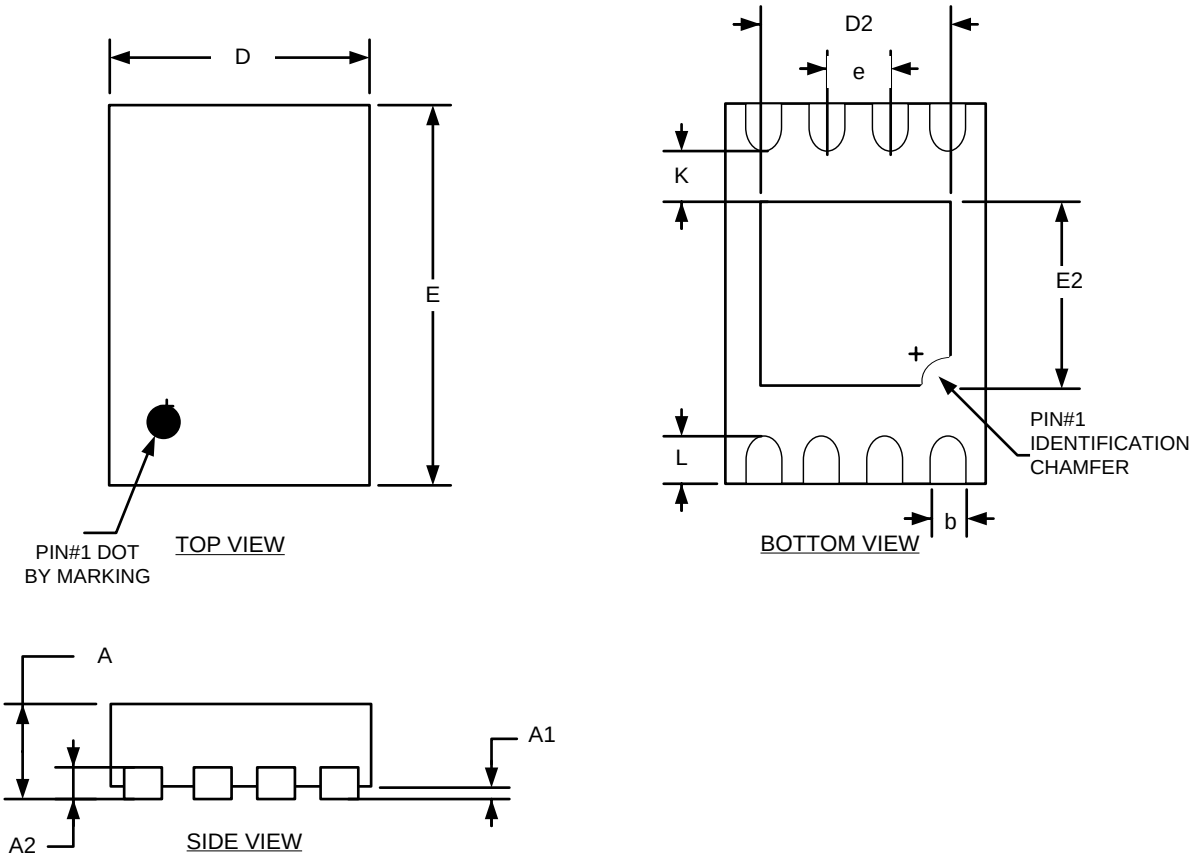




Note:
1. Controlling Dimension:MM
2. Dimension D and E do not include Mold protrusion
3. Dimension b does not include dambar protrusion/intrusion
4. Refer to Jedec standard MO-153 AA
5. Drawing is not to scale
6. Package may have exposed tie bar.

| SYMBOLS | DIMENSIONS IN MILLIMETERS | | | DIMENSIONS IN INCHES | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | -- | -- | 1.20 | -- | -- | 0.047 |
| A1 | 0.05 | -- | 0.15 | 0.002 | -- | 0.006 |
| A2 | 0.80 | 1.00 | 1.05 | 0.031 | 0.039 | 0.041 |
| b | 0.19 | -- | 0.30 | 0.007 | -- | 0.012 |
| c | 0.09 | -- | 0.20 | 0.004 | -- | 0.008 |
| D | 2.90 | 3.00 | 3.10 | 0.114 | 0.118 | 0.122 |
| E | 4.30 | 4.40 | 4.50 | 0.169 | 0.173 | 0.177 |
| E1 | 6.4 BSC | | | 0.252 BSC | | |
| e | 0.65 BSC | | | 0.026 BSC | | |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| Θ | 0 | -- | 8° | 0 | -- | 8° |

## 10.3 UDFN

### 8L 2x3mm UDFN Package Outline




| SYMBOLS | DIMENSIONS IN MILLIMETERS | | | DIMENSIONS IN INCHES | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.50 | 0.55 | 0.60 | 0.020 | 0.022 | 0.024 |
| A1 | 0.00 | -- | 0.05 | 0.000 | -- | 0.002 |
| b | 0.18 | 0.25 | 0.30 | 0.007 | 0.010 | 0.012 |
| A2 | 0.152 REF | | | 0.006 REF | | |
| D | 2.00 BSC | | | 0.079 BSC | | |
| D2 | 1.25 | 1.40 | 1.50 | 0.049 | 0.055 | 0.059 |
| E | 3.00 BSC | | | 0.118 BSC | | |
| E2 | 1.15 | 1.30 | 1.40 | 0.045 | 0.051 | 0.055 |
| e | 0.50 BSC. | | | 0.020 BSC. | | |
| K | 0.40 | -- | -- | 0.016 | -- | -- |
| L | 0.20 | 0.30 | 0.40 | 0.008 | 0.012 | 0.016 |

Note:

1. Controlling Dimension:MM
2. Drawing is not to scale

## 11. Revision History

| Revision | Date | Descriptions |
|---|---|---|
| A0 | Feb. 2023 | Initial version |
| | | |